

CUSTOMER NO.: 24498
Serial No. 10/590,555
Office Action dated: 12/08/10
Response dated: 04/08/11

PATENT
PD040028

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Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Please cancel claims 2 and 7-10 without prejudice.

Please amend claims 1, 3 and 11 as follows:

1. (Currently Amended) Arrangement for adaptive bit recovery, comprising: including
an adaptive equalizer; and
an adaptive partial response maximum likelihood detector; ~~wherein the~~
~~arrangement further includes~~
an overflow control block for the adaptive equalizer for monitoring one or more of the adaptation coefficients; and
a scaling block for applying a scaling to one or more data paths of the coefficients when the overflow control block indicates that one or more of the coefficients is out of an intended data range, wherein the scaling is applied such that a middle coefficient has the highest value.
2. (canceled)
3. (Currently Amended) Arrangement according to claim 1, further including means for obtaining phase information by comparing ~~the~~ a highest absolute coefficient value with its coefficient number.
4. (Previously Presented) Arrangement according to claim 1, further including a control logic for an adaptation constant for a tap value update for the coefficients.

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5. (Previously Presented) Arrangement according to claim 4, further including a gradient analyzing block for analyzing a gradient of the coefficient transitions for monitoring the speed of adaptation.
6. (Previously Presented) Arrangement according to claim 5, further including a set level block for performing an adaptation coefficient scaling in dependence on the value of the detected gradient.
7. (canceled)
8. (canceled)
9. (canceled)
10. (canceled)
11. (Currently Amended) Arrangement according to claim 1, wherein generated error information is provided to ~~further~~ processing units for supporting data processing.
12. (Previously Presented) Apparatus for reading from and/or writing to recording media, wherein it includes an arrangement according to claim 1 for adaptive bit recovery.